

FIG. 1 (Prior Art)

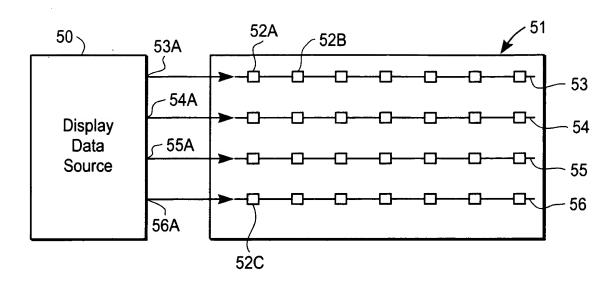
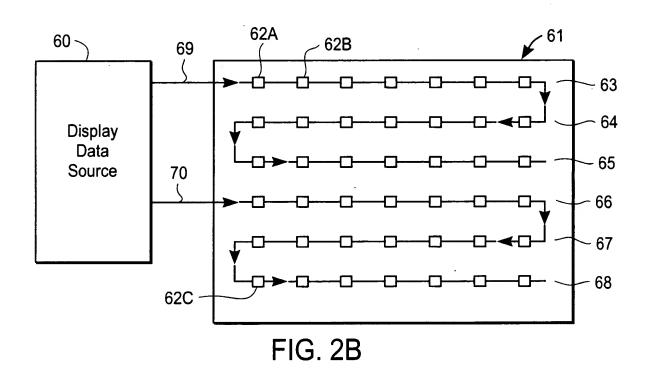


FIG. 2A



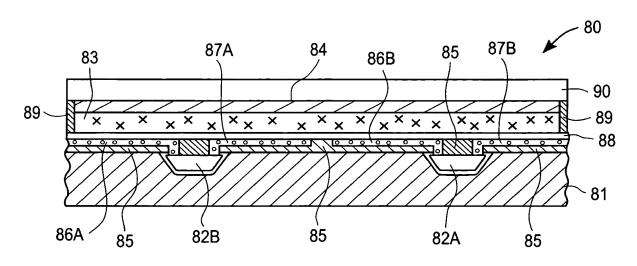


FIG. 2C

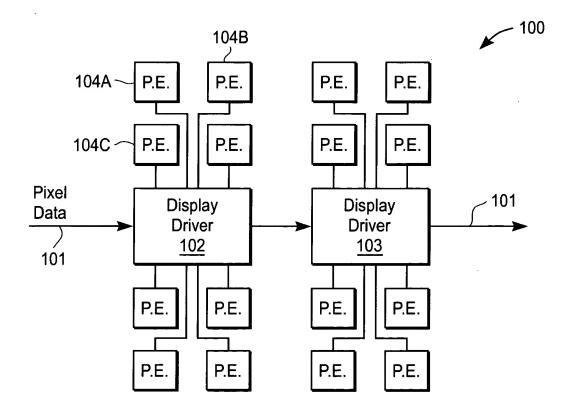
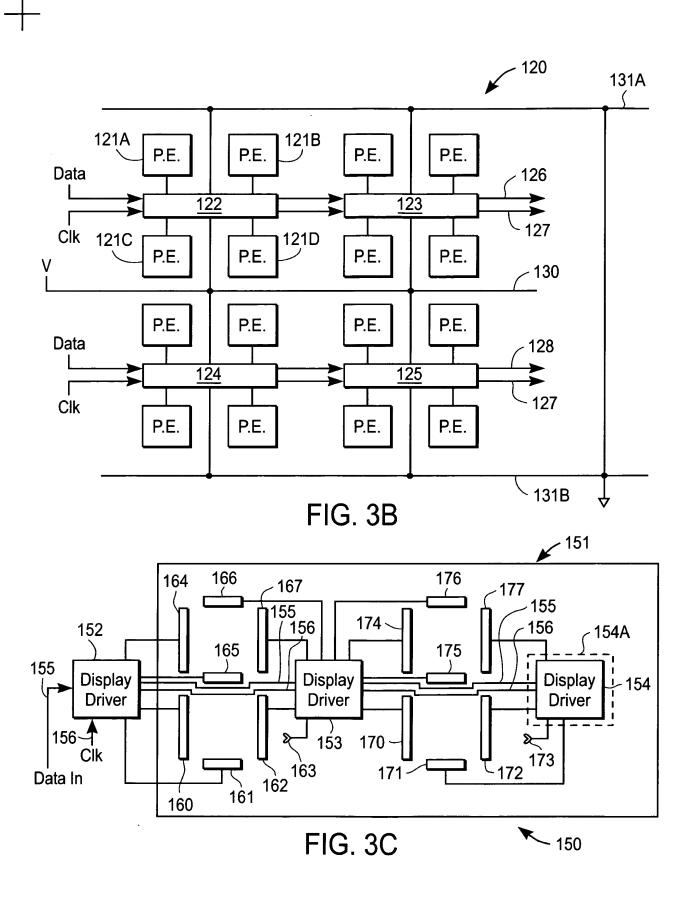
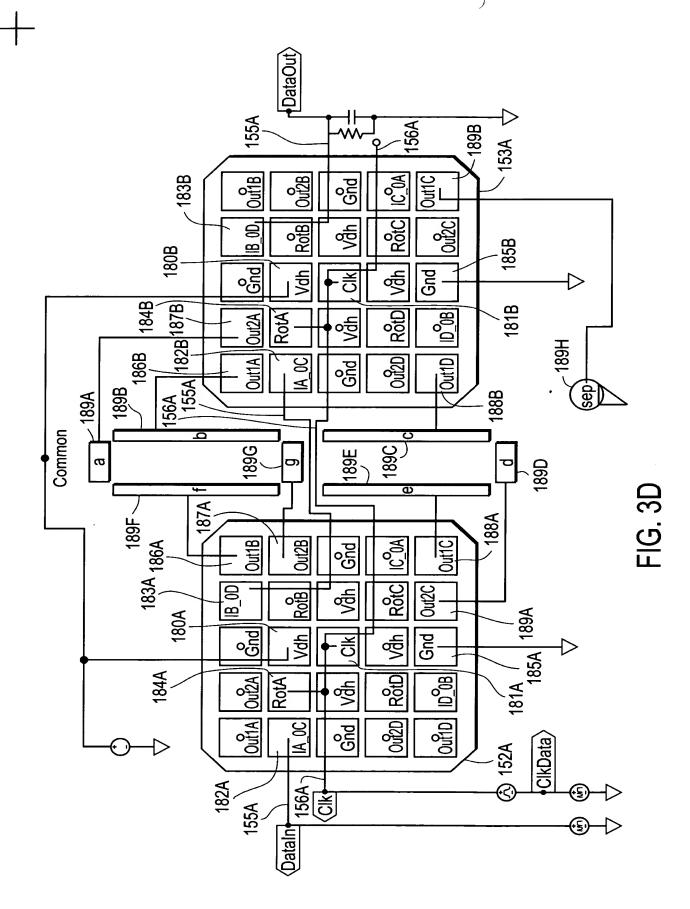
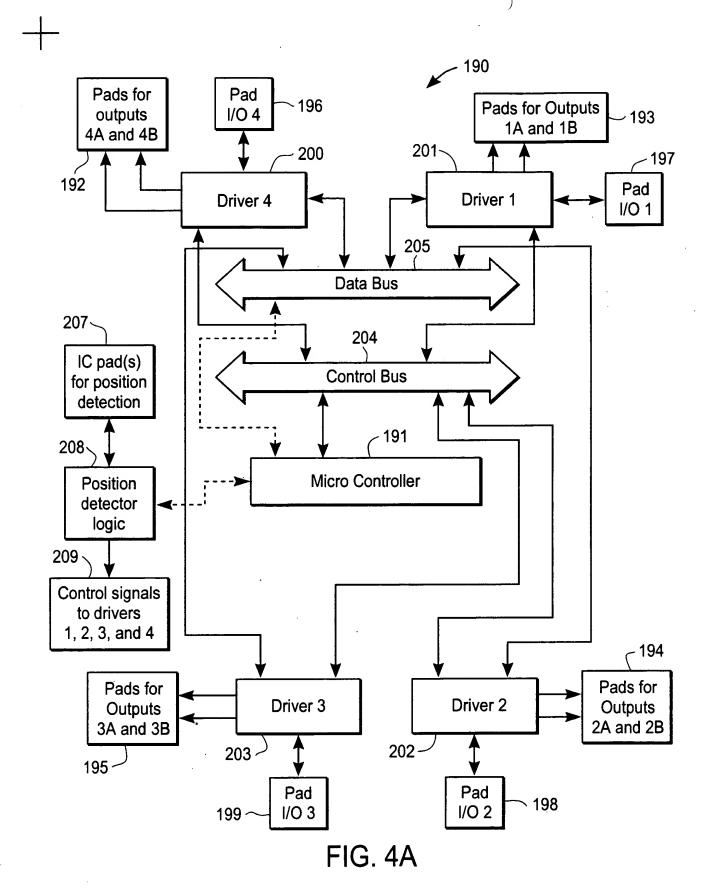


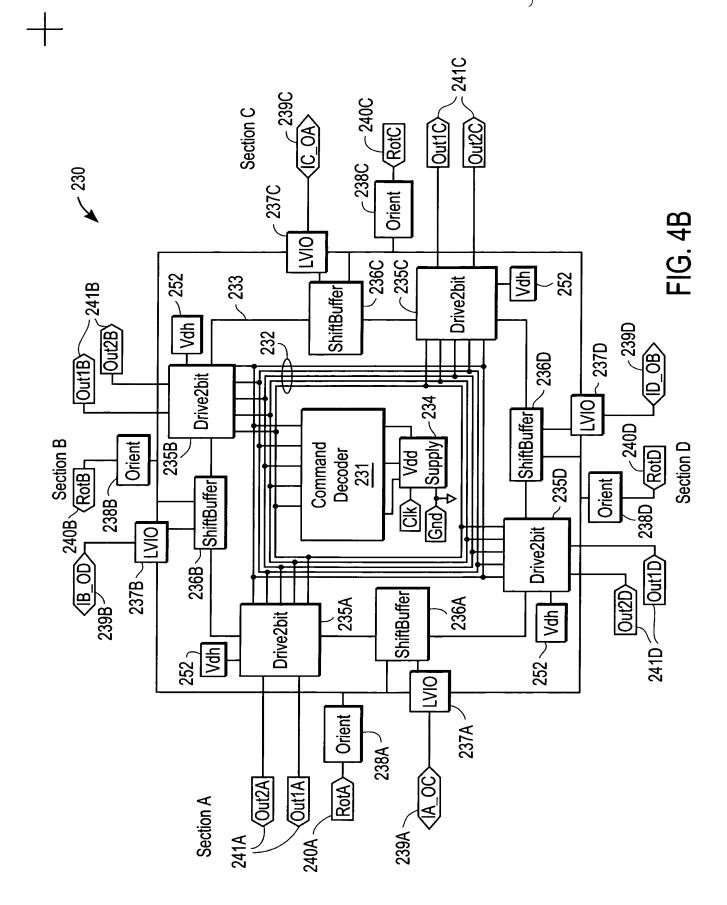
FIG. 3A

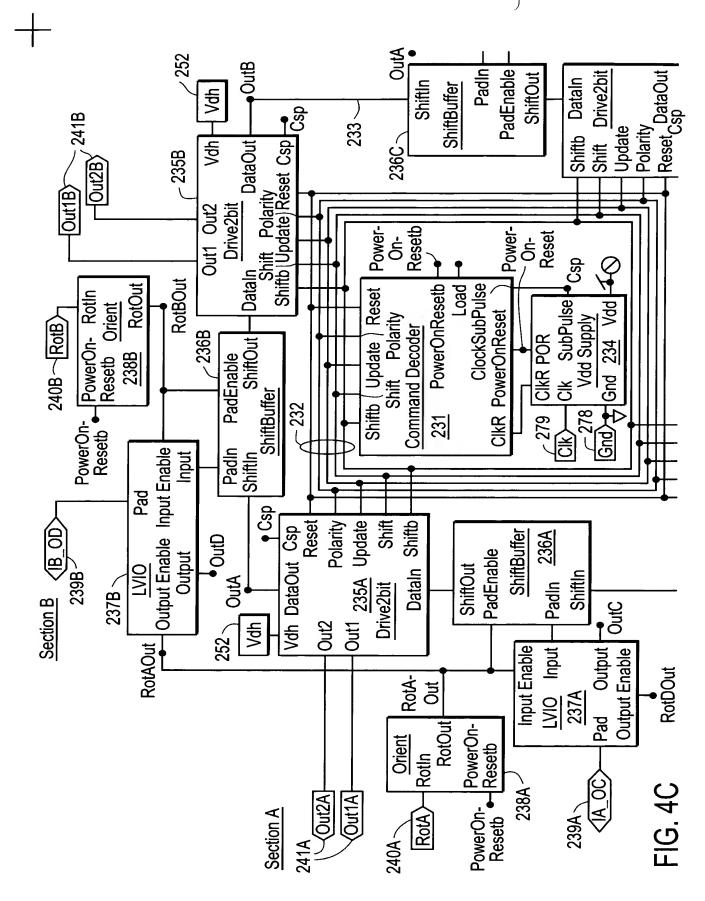




+







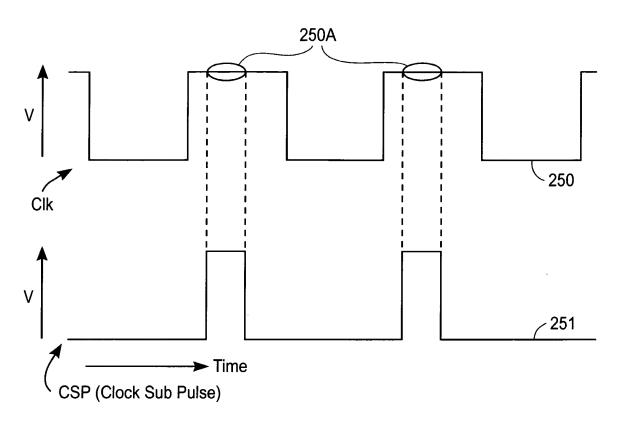
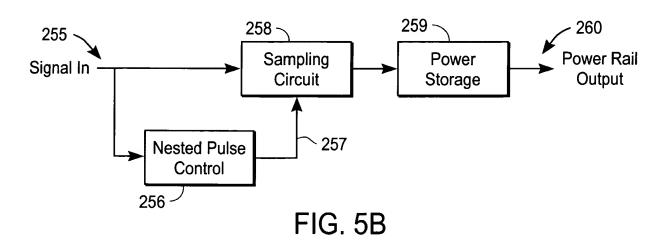
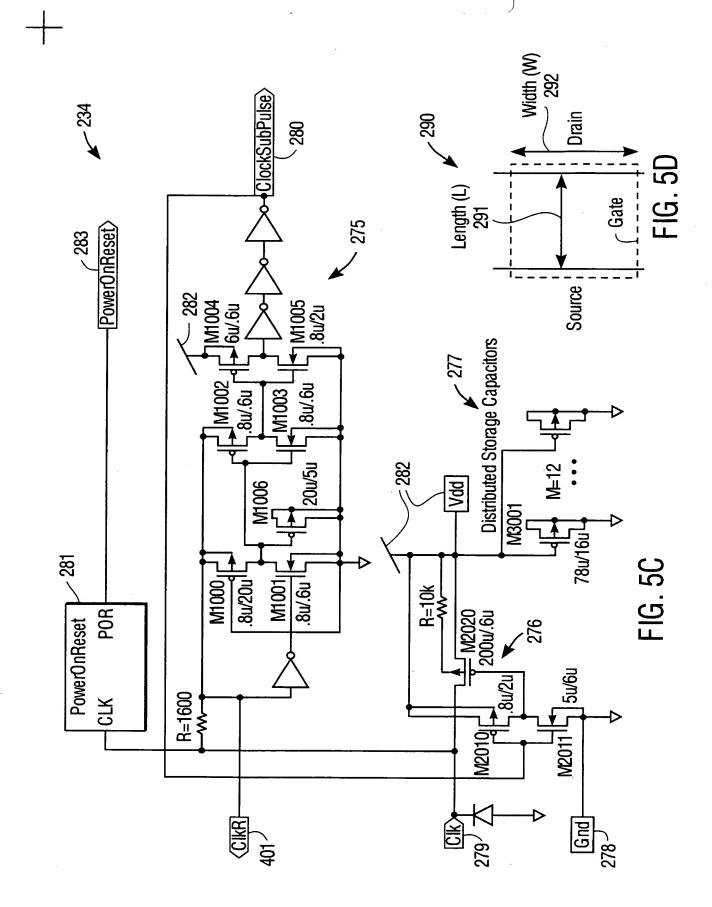
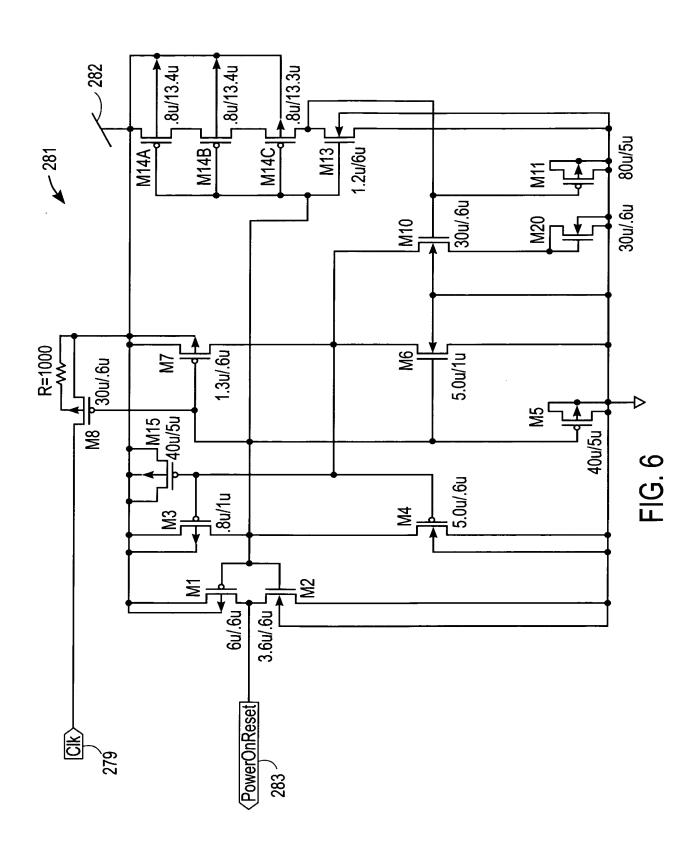


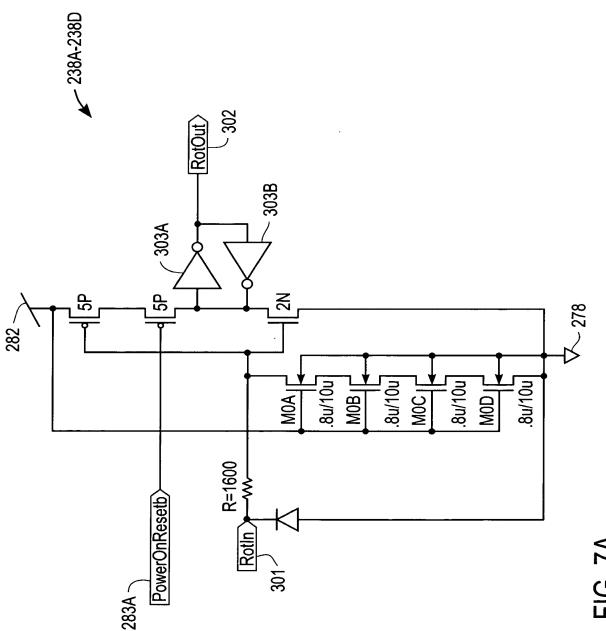
FIG. 5A











-15. /A

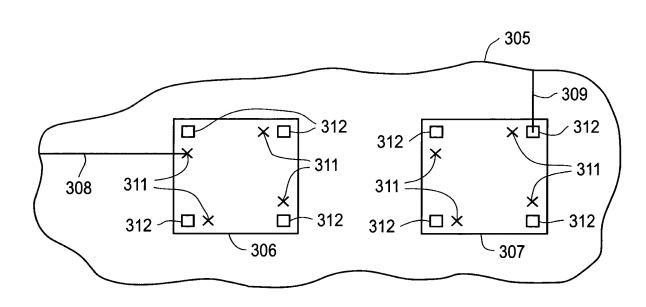


FIG. 7B

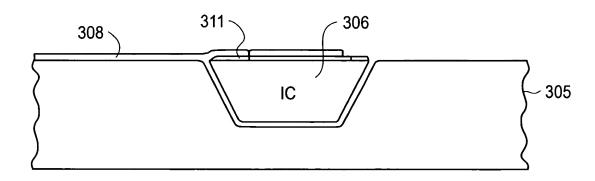


FIG. 7C

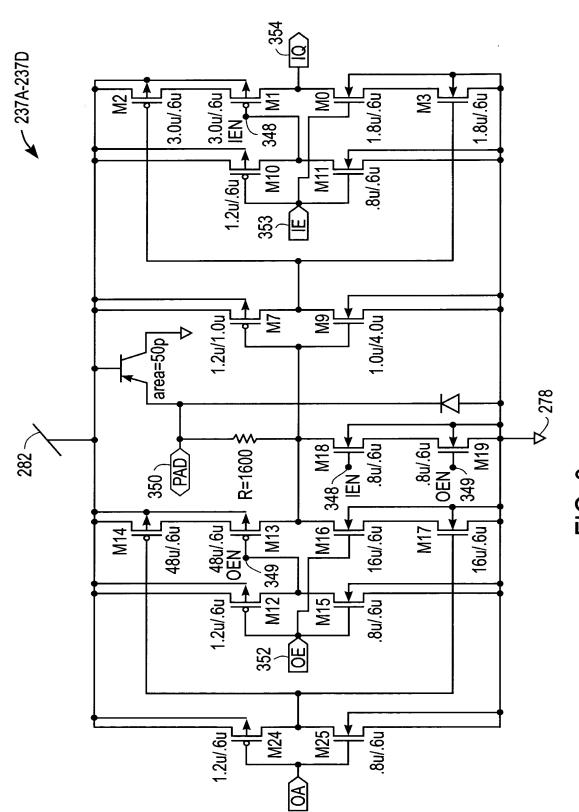
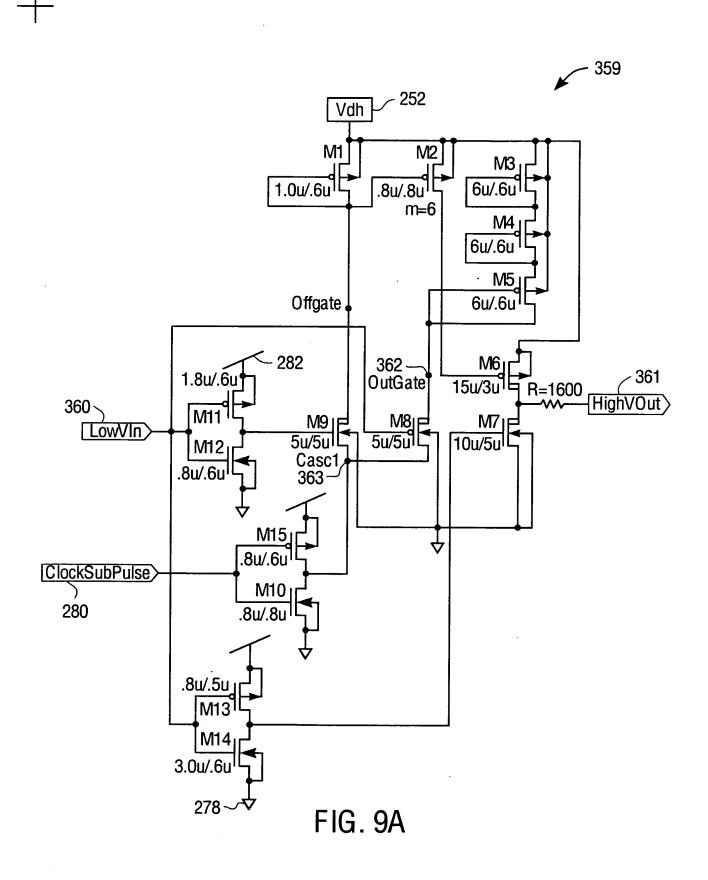
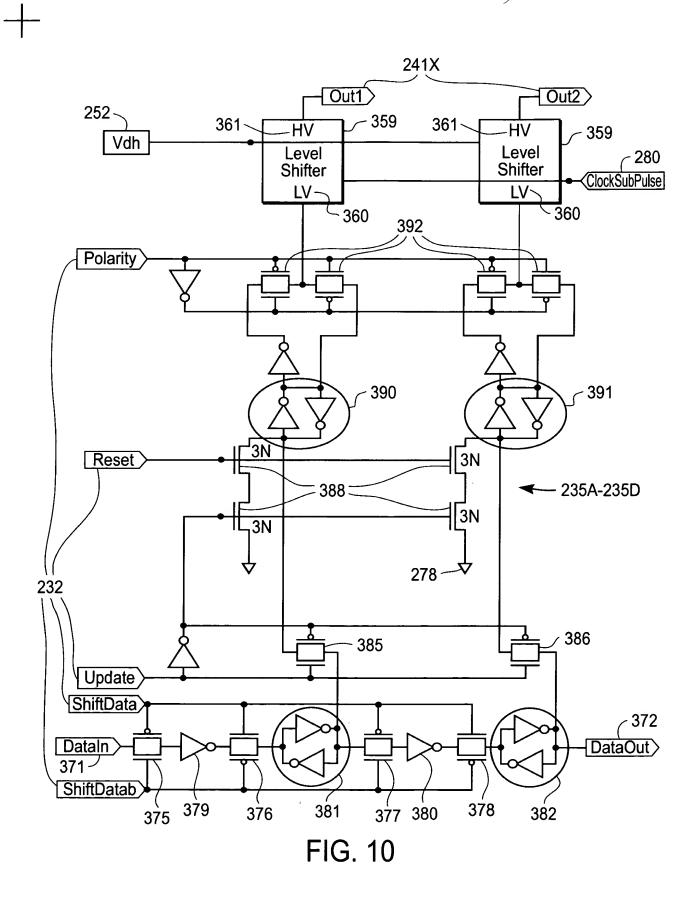
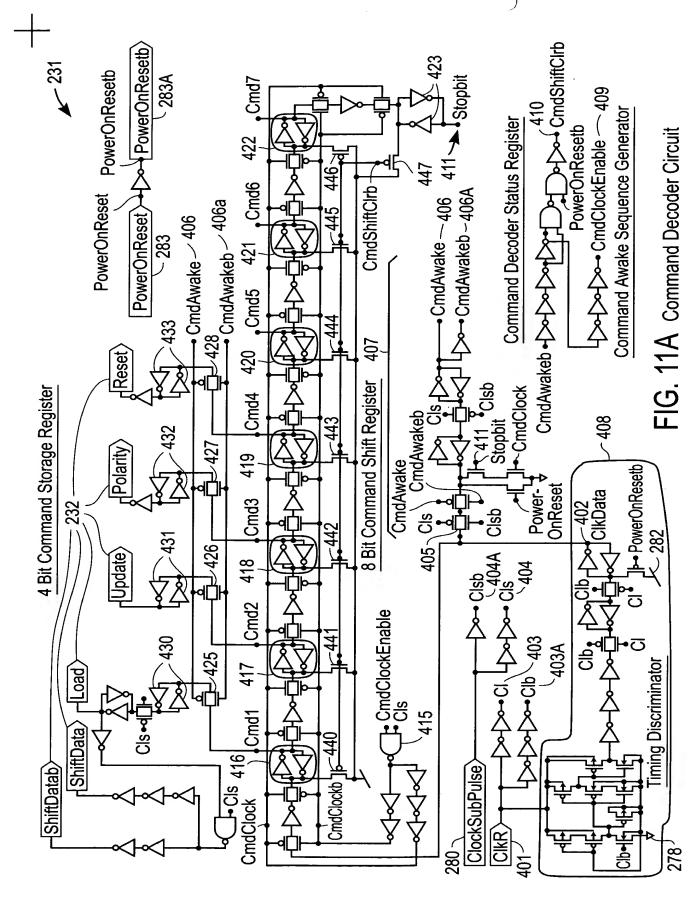
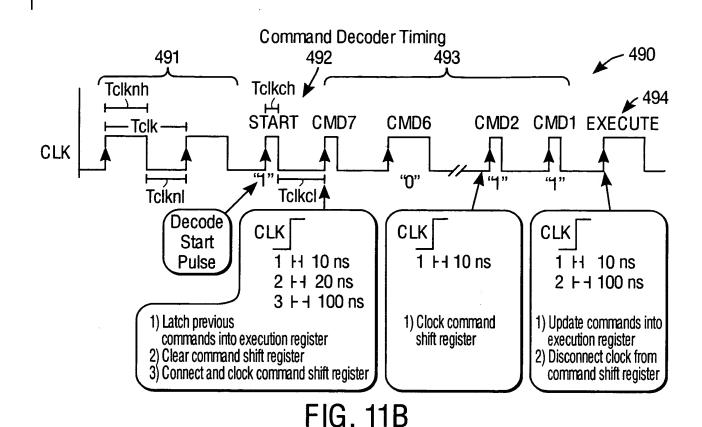


FIG. 8

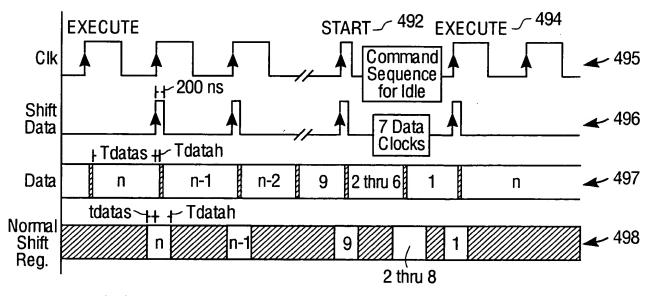








Data Load Timing



- n is the total number of data values for all daisy-chained device blocks. (example: n = 32 for 4 device blocks).
- data must be low upon start-up and through the first command sequence.

FIG. 11C

501 Timing Discriminator determines that it has received a short clock pulse and ClkData goes "high" (= "1") indicating header bit of command/ instruction has been received 502 CmdAwake signal goes high after ClkData goes high and Command Storage Register (formed by inverter pairs 430, 431, 432, and 433) is disconnected from Command Shift Register (formed by inverter pairs 416-423) 503 Old instruction data in Command Shift Register is cleared to low ("0") with assertion of CmdShftClrb (when CmdShftClrb goes low ("0"), and CmdClockEnable is generated/asserted and this allows the clock signal named CmdClock to be provided through Command Shift Register 504 Every clock cycle thereafter (until header "1" bit reaches inverter pair 423) shifts instruction bits through the Command Shift Register (short clock cycle = high ("1") and long clock cycle = low ("0") 505 When header bit reaches last stage (inverter pair 423) stop bit signal is asserted, which stops the shifting (CmdClockEnable is deasserted), and CmdAwake goes low causing the Command Shift Register to update the Command Storage Register

FIG. 11D

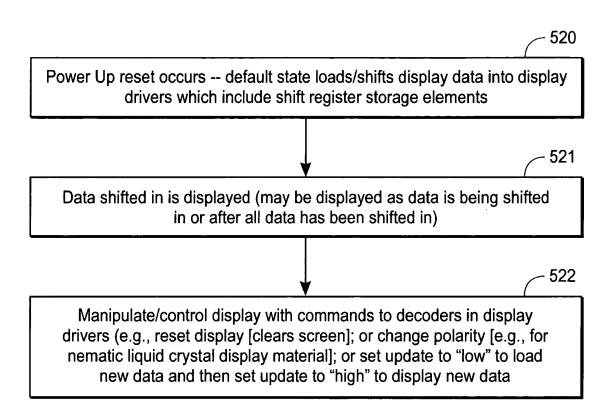
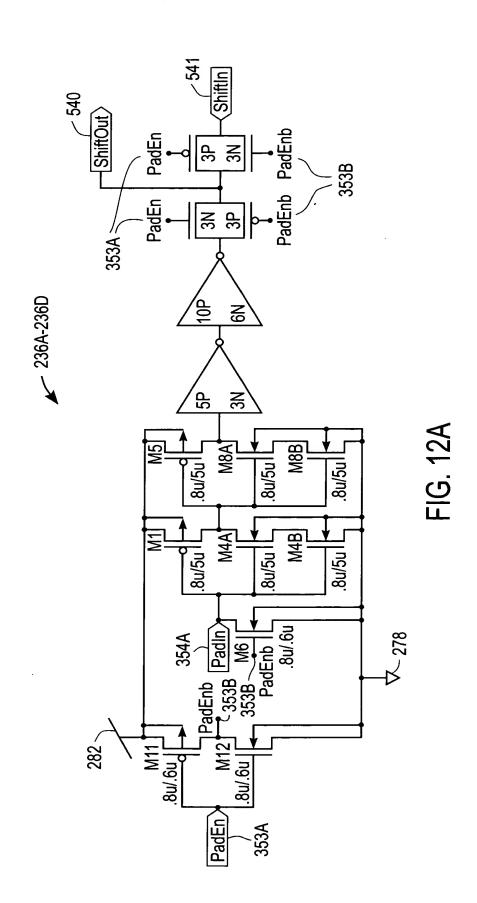
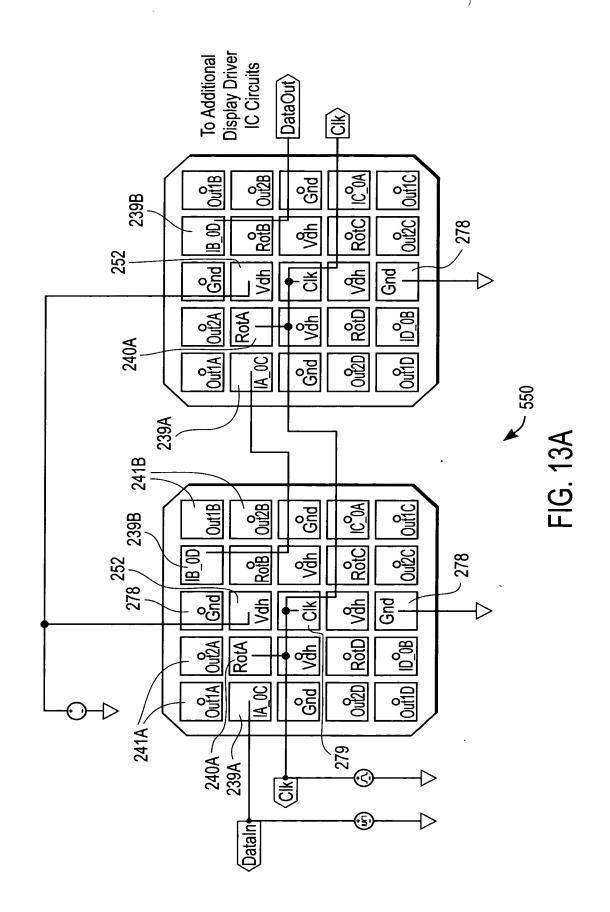
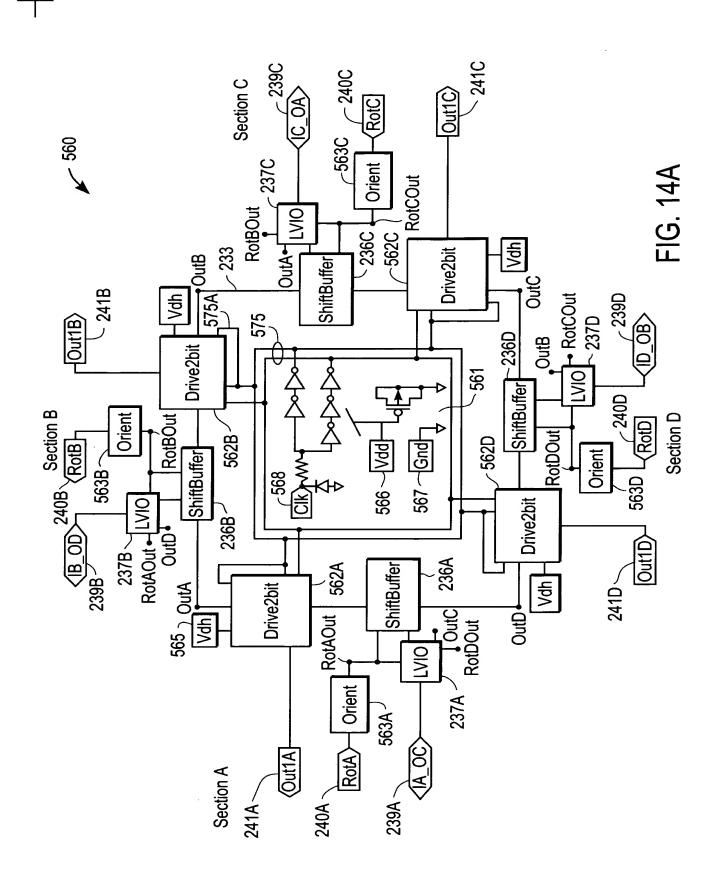


FIG. 11E







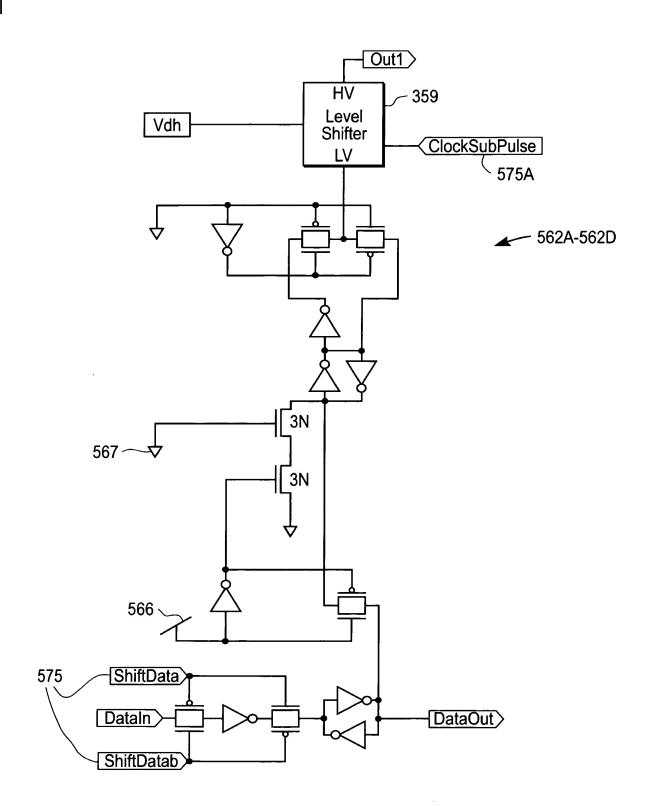


FIG. 14B

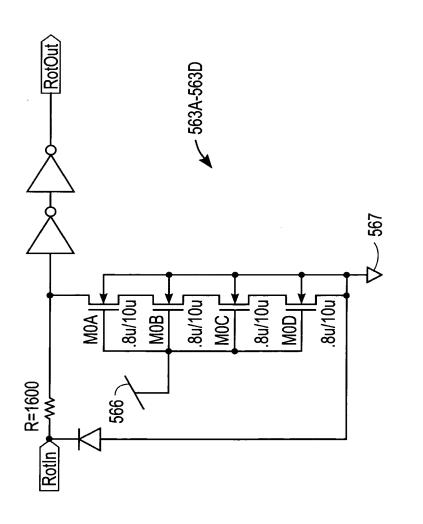


FIG. 14C

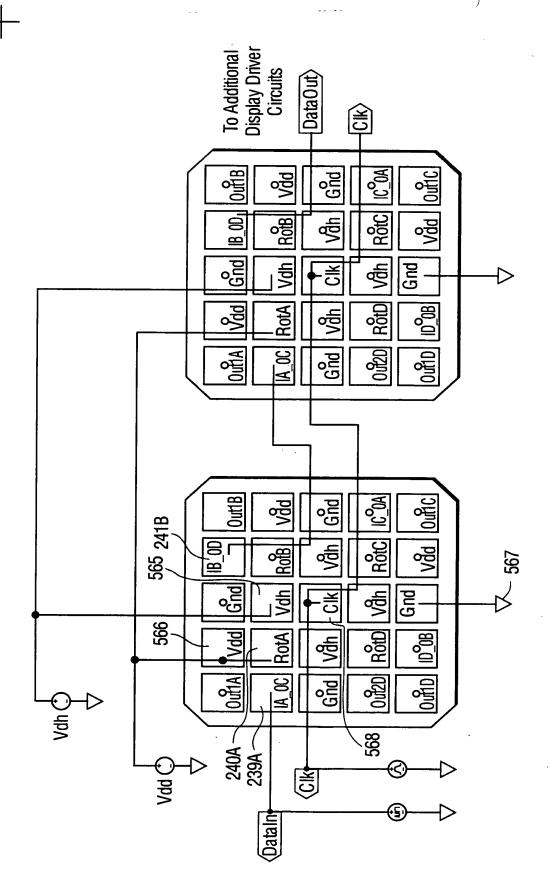


FIG. 14D

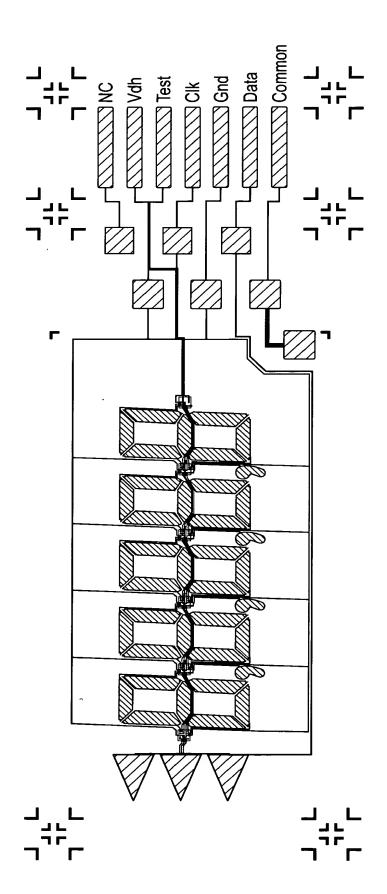


FIG. 15A

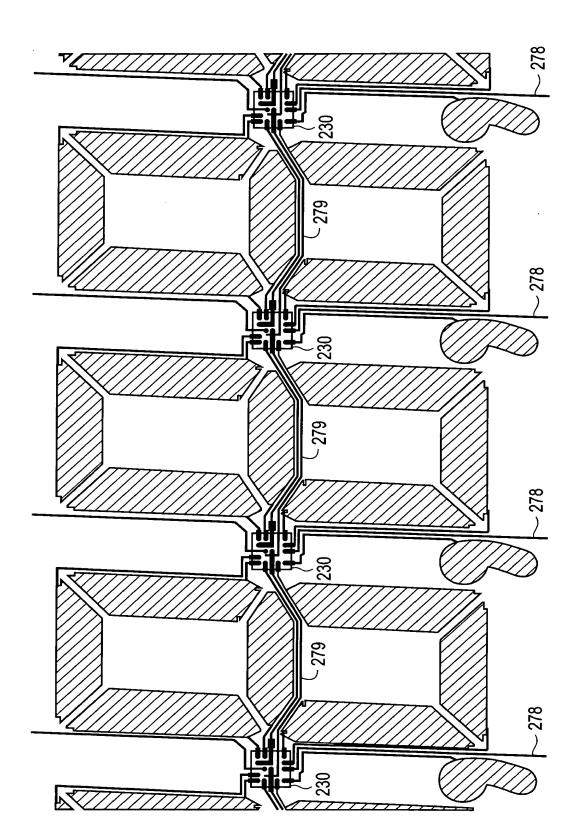


FIG. 15B